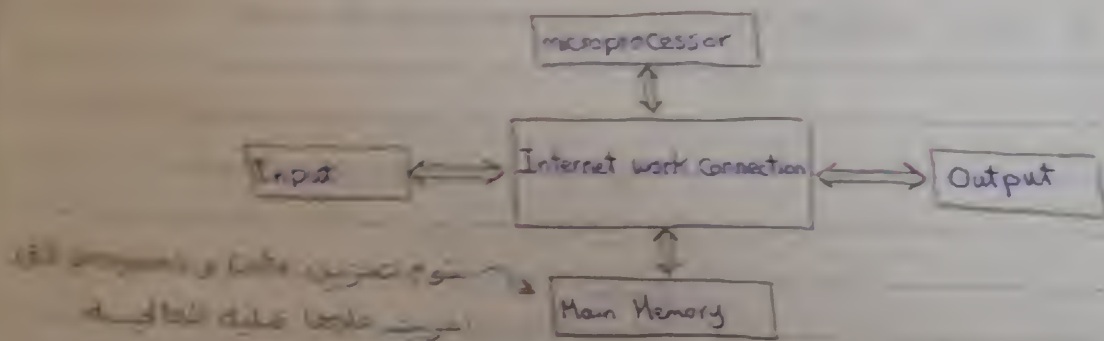
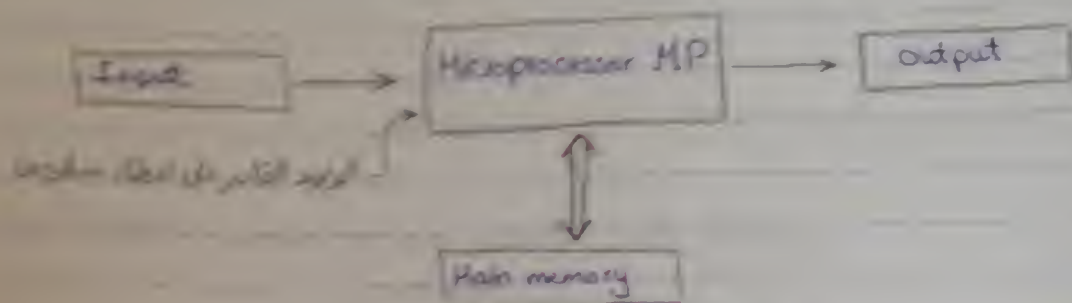
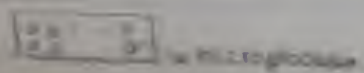


Ch 1 Microprocessor (Introduction)



Central processing Unit (CPU) \equiv Machine



→ CPU components

1. ALU

2. CU (Control Unit)

3. Registers and Cache

نظام في ذاكرة المعالج

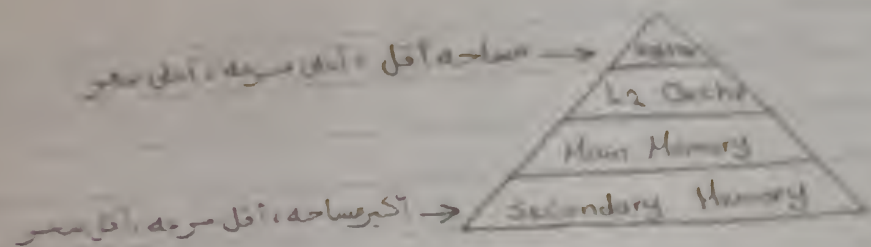
→ CPU Functions:

1. ~~Exec~~code arithmetic & logic instruction
(Fetch - decode - execute)

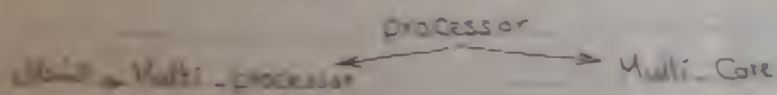
→ Manage the program Flow (make decisions)

* Zero * negative * overflow ...

- 1 -



→ Transfer Data between itself and memory



Bus: group of common wires connect between parts of device.

1) Address Bus :

K-bit → 2^K devices

2) Data Bus :

devices ↔ MP



← کما زاد کما زاد نقل البيانات من وإلى MP

3) Control Bus :

devices ↔ MP



← Control Signal

کما زاد کما کان أفضل

Draw the block diagram of a computer system showing the address, data and control bus signal?



→ Simple Control Signal

MWIC memory write control signal
 MRDC memory read control signal
 IOWC I/O write control signal
 IORC I/O read control signal

→ MP → device القاعل بين

- 1- MP → send address
- 2- Control signal MRDC
- 3- Data transfer.

The memory system is divided into 3 main parts:

1. Transient program area (TPA)
2. System Area
3. Extended memory system (EMS)

1.

- holds
- The length of TPA is 640 KB
- programs → interrupt vector

Ch2 : The Microprocessor & Its Architecture

8 bit	16 bit	8 bit	
AH	AX	AL	Accumulator
BH	BX	BL	Base Index
CH	CX	CL	Count
DH	DX	DL	Data
	SP		Stack Pointer
	BP		Base Pointer
	DI		Destination Index
	SI		Source Index

IP
FLAG

CS	Code Segment
DS	Data Segment
ES	Extra Segment
SS	Stack Segment
FG	
GS	

special purpose.

Programming Model of The Intel 8086 Pentium 4

32 bit	8bit	16bit	32bit	
EAX	AX	AX	AL	Accumulator
EBX	BX	BX	BL	Base Index
ECX	CX	CX	CL	Count
EDX	DX	DX	DL	Data
ESP		SP		Stack Pointer
EBP		BP		Base Pointer
EDI		DI		Destination Index
ESI		SI		Source Index

	IP	Instruction Pointer
	FLAGS	Flags

CS	Code
DS	Data
ES	Extra
SS	Stack
FS	
GS	

The Programming Model OF The Intel 386 Pentium 4

كل 4 bit في الثنائي يعطى 1 bit في السادس عشر
 20 bit → (xxxxx) Hexa.

Real Mode

Segment	Off Set	Special Purpose
CS	IP - EIP	Instruction address
SS	SP - BP ESP / EBP	Stack address
DS	BX - DI - SI Data numbers	Data address
ES	DI - EDI String Instructions	String destination address
FS - GS	No default	General address

Flag Register Model

program Visible

- They are used during app - prog
- ex: EAX, AX, AL, EBX, ...
- Mov AX, BX

program invisible

- not addressed directly during app - prog
- only 80286 - P4
- Contain this type
- ex: FLAG, EFLAG
- SUB AX, BX بعد تنفيذ أمر

Purpose of use

General purpose

EAX, EBX

Hold Data address or offset +

المحتوى على الذاكرة

int x = 3
↑ ↑
address data

Special purpose
CS, DS, ES, SS

Addressing modes (How the memory is accessed)

Addressing mode ← أكثر بكثير طرق تنظيم البيانات داخل الذاكرة
وطريقة الوصول إلى الذاكرة

- 1 - Real mode 1 MB only
- 2 - Protected mode upto 4GB

« Real mode »

→ Accumulator EAX, AX, AL, AH

Can be used as 32 bit → EAX, 16 → AX, 8 bit → AH, AL

II Special purpose.

← طرق أساسية في عمليات الضرب والقسمة

→ Div AX, BX : $\frac{AX}{BX}$

AX: يوضع له الجزء الصحيح

DX: (Data register) يوضع به باقي القسمة "الكسر"

→ Mux AX, BX

16 * 16 → 32 bit

→ Mux EAX, EBX

32, 32

DX
high bytes

AX
low bytes

EDX
high bytes

EAX
low bytes

Base Index

Can be used as 32 bit \rightarrow EBX, 16 bit \rightarrow BX
8 bit \rightarrow BH, BL

General purpose \rightarrow hold offset for Data Segment

Note: In Real Mode

We have 8086 processor, 5 bit memory

\rightarrow To access the memory
الموصول للذاكرة
 \leftarrow processor - CPU

$$64K = 2^6 \cdot 2^{10} = 2^{16}$$

(16 bit) \rightarrow (4 bit) Hex.

\rightarrow From 4 bit processor how to reach 5 bit memory

we add zero from the left side to Base

\rightarrow To reach to any address in the memory we need Base and offset

الـ Base is in Code Segment

$$\text{Current address}_{(\text{real})} = (\text{CS})_0 + \text{offset}$$

$$\text{EX: } \text{CS} = 4000 \text{ Hex}, \text{ IP} = 2342$$

Solution

$$\text{Current address} = (\text{CS})_0 + \text{IP} = 40000 + 2342 = 42342 \text{ Hex}$$

Count

To Count in any process with loop we need big register

loop CX, ECX

Repetition CX

Shift CL

we need small number of loops

Data

Can be used as 32 bit \rightarrow EDI 16 bit \rightarrow DX
8 bit \rightarrow DI, DL
General purpose \rightarrow DI, DX لغزب والقسمه

Stack pointer

Can be used as 16 bit \rightarrow SP
hold the offset of stack segment (SS) \leftarrow الأولويه له

Base pointer

Can be used as 16 bit \rightarrow BP
used as offset for stack segment (SS)

Destination Index

Can be used as 16 bit \rightarrow DI له الأولويه بعد DI
hold the offset of Data segment

Source Index

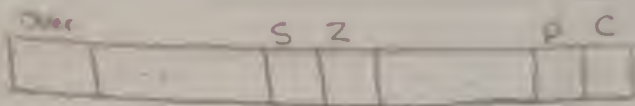
Can be used as 16 bit \rightarrow SI له الأولويه بعد DI
hold the offset of Data segment

Instruction Pointer

Can be used as 16 bit \rightarrow IP
hold the offset of current instruction to be executed (in Code segment)

Ch 4 : Data Movement Instructions

Flag - invisible



Can be used as 16 bit - 32 bit

→ Help microprocessor to take the correct way

① Over Flow happened when

$$\begin{aligned} &\rightarrow +VE + +VE = -VE \\ &\rightarrow -VE + -VE = +VE \end{aligned}$$

② Carry (C)

1111010
Carry 1111101+
② ← 1101001

③ Parity (P)

1 → number of one's is even

0 → number of one's is odd

نستفيد من هذا عندما يتم نقل Data من مكان لآخر نتأكد من أن Data تم نقلها دون فقد صيغة إذا كان عدد 1 وريوس عدد النقل وخالصه Parity فان النقل تم بالصورة المطلوبة وانعكس يكون فيه فقد في Data

Ex: SS = 3245 H

BP = 2342

Sol

Base address = 33450 H

Current address = 33450 + 2342 = 35792

Ending address = Starting + FFFF
= 33450 + FFFF

- 7 -

Used in two dimension . . .

Ch 3 Addressing modes (Blind Model)

[I] Immediate Addressing Mode

I → R

↑
Register

Examples

Mov BL, 44
Mov CL, 1001110 B
Mov ECX, FC23F34EH



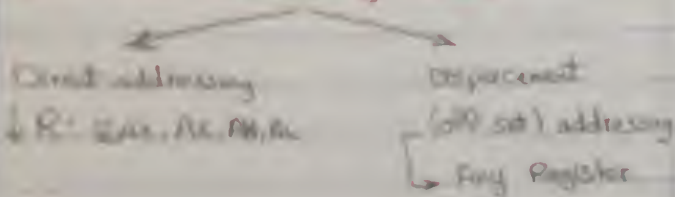
[II] Register Addressing Mode

R ↔ R

↑
Register

Mov CL, BL
Mov CX, BX
Mov EAX, EBX
Mov DS, CX
Mov DS, CS

[III] Direct Addressing Mode



R ↔ M

↑
memory

Direct Displacement
Mov AL, Num
Mov AX, Num
Mov Num, AX
Mov EAX, Num

Displacement
Mov CL, Num
Mov CX, Num
Mov EBX, Num
Mov DX, [1023]

[IV] Register Indirect Addressing Mode

(BP, BX, SI, DI)

R ↔ []

Mov AX, [BX]
Mov [BP], DL
Mov EDI, [DI]
Mov [BX], [ESP] (X)



[V] Base Plus Index Addressable Mode

EBX → BX
ESI → SI
EDI → DI
use with one dimension array

R ↔ M

Mov DI, [BX + DI]
Mov WORD PTR [BX + DI], DX

[VI] Register Relative Addressable Mode

EBP → BP
ESI → SI
EDI → DI
offset

R ↔ M

Mov AX, [BX + 1000]
Mov AX, 1000 [DI]
Mov WORD PTR [BX + 1000], AX

[VII] Base relative plus index Addressable Mode

Used in Two dimension Array

R ↔ M

Mov WORD PTR 1000 [BX + DI], A
Mov DH, [BX + DI + 20h]

Effective Address (EA)

No EA

$R_{source} (R_s)$

Register الذي يحصل منه على البيانات

$$EA = memory = Num$$

Notes

(16) عشري
(8) ثنائي
(32) ثنائي عشر

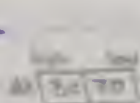
$R \rightarrow R$ has the same size

لا يجوز أي حال من الأحوال تغيير segment Code (CS) الذي يحتوي على عنوان الذاكرة وأمر داخل الذاكرة ولذلك لا يجوز النقل من segment إلى آخر

1 → Memory ~ Byte addressable

عزقة بـ Byte by Byte

2 →



little endian arrangement

$$EA = (seg)_0 + \text{offset}$$

$$\textcircled{1} EA = (DS)_0 + BX$$

$$\textcircled{2} EA = (SS)_0 + BP \quad \textcircled{3} EA = (DS)_0 + DI$$

$$EA = (DS)_0 + BX + DI$$

starting address

$$EA = (DS)_0 + BX + 1000$$

$$EA = (DS)_0 + \begin{matrix} BX \\ DI \\ 1000 \end{matrix}$$

عند نقل بيانات من Register إلى Memory لابد من تحديد المساحة المطلوب تخزين البيانات بها حيث أن

Memory byte addressable

Mov [BX], AL

لديهم قيد مساحة التخزين

لديهم التخزين إلى

Mov Byte PTR [BX], AL

Mov Word PTR [BX], AL

Mov DWord PTR [BX], AL

effective address

ويظل

عند نقل بيانات من Memory إلى Register لا حدد

المساحة للتخزين ولا توجد مشاكل

Ch 4: Data Movement Instructions

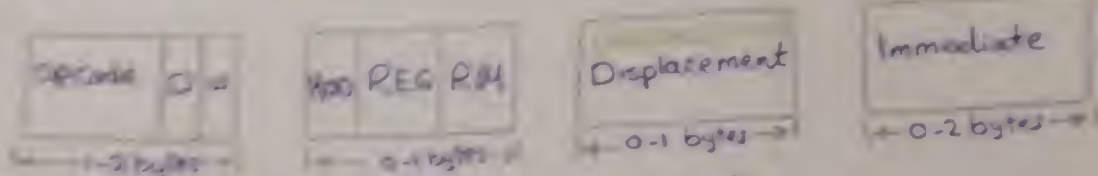
1. Assembler & Disassembler
2. Stack (push, pop)
3. Instructions

Assembler & Disassembler

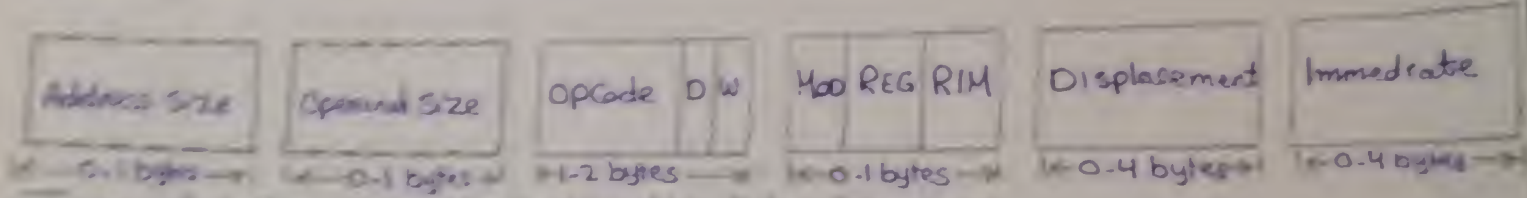
Header: number, number, to memory
code, to memory, code
Operand: number, number
code, to memory, code

Modes of Instruction

1. 16 bit instruction mode (8086)



2. 32 bit instruction mode (80386 above)



To translate from assembler to disassembler follow this steps

III

Operand Size	Address Size	mode
<p>64 bit</p> <p>X</p>	<p>64 bit</p> <p>X</p>	<p>- 16-bit instruction mode with its default (8 - 16 bit) registers</p>
<p>✓</p>	<p>X</p>	<p>- 16 bit instruction but works with (8 - 32 bit) registers.</p>
<p>X</p>	<p>✓</p>	<p>- 32 bit instruction works with its default (8 - 32 bit) register</p>
<p>✓</p>	<p>✓</p>	<p>- 32 bit instruction but works with (8 - 16 bit) registers.</p>

2

Op-Code	0	1
---------	---	---

→ Op-Code: Two machine code of the instruction (Mov, Sto, push)
we get this code from the table
1111 1111 → 100010

→ 0 → Dest (When we transfer from Memory to register)
→ 1 → Src (When we transfer from register to Memory)

→ W → W=1 (Word / Double)
→ W=0 (Byte)

3

MOD	REG	R/M
-----	-----	-----

→ MOD: Its machine code can be get from this table

MOD	Function	Ex:
00	No Displacement	Mov AL, [EDI]
01	8-bit sign-extended displacement	Mov AL, [EDI+2]
10	16-bit displacement	Mov AL, [EDI+1000h]
11	R/M is a register	

→ REG: Its machine code can be get from this table

Code	W=0 (Byte)	W=1 (Word)	W=1 (Double)
000	AL	AX	EAX
001	CL	CX	ECX
010	DL	DX	EDX
011	BL	BX	EBX
100	AH	SP	ESP
101	CH	BP	EBP
110	DH	SI	ESI
111	BH	DI	EDI

Code	Seg
000	ES
001	CS
010	SS
011	DS
100	FS
101	GS

→ R/M → to get the code of R/M read first we want to know if R/M is memory or Register that depend on MOD


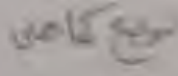
IF MOD = 11 & R/M is registers
we can get its code from register table.

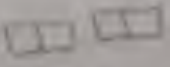
Code	W=0 (byte)	W=1 (word)	W=10 (double)
000	AL	AX	EAX
001	CL	CX	ECX
010	DL	DX	EDX
011	BL	BX	EBX
100	AH	SP	ESP
101	CH	BP	EBP
110	DH	SI	ESI
111	BH	DI	EDI

IF MOD = (00, 01, 10) & R/M is Memory
we can get its code from this table

R/M Code	Addressing mode	Function
000	DS: [BX + SI]	DS: [EAX]
001	DS: [BX + DI]	DS: [ECX]
010	SS: [BP + SI]	DS: [EDX]
011	SS: [BP + DI]	DS: [EBX]
100	DS: [SI]	uses scaled-index byte
101	DS: [DI]	SS: [EBP]*
110	SS: [BP]* <small>special addressing mode</small>	DS: [ESI]
111	DS: [BP]	DS: [EDI]
	16-bit R/M memory addressing mode	32-bit addressing mode selected by R/M

④ Displacement

① 1 byte  → put as it is 
ex: 1 → 01 21 → 21

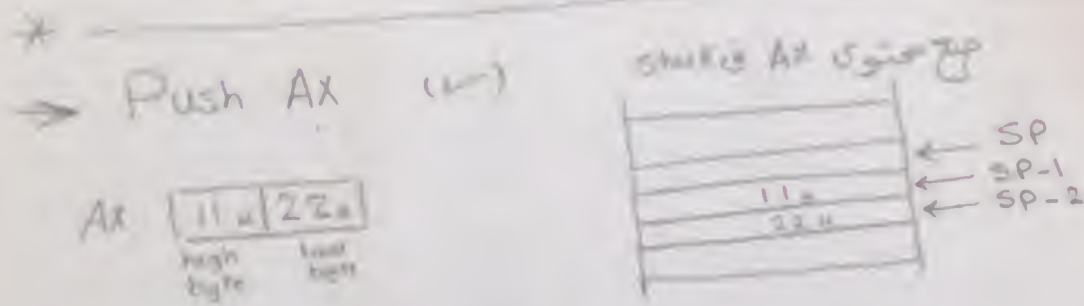
② 2 byte  → swap high, low

ex: 1234 → 3412

ex: 23 → 2301

Stack (pop & push)

→ The PUSH and POP instructions are important instructions that store and retrieve data from the LIFO (last in first out) stack memory



→ push B262h (✓)

→ push [Bx] (x) ← هيا لم يرد الفصاحة التي
يخزن بها البيانات في memory

$$EA = (DS)_0 + BX$$

The correct

push byte PTR [Bx] (✓)

push (word - Dword) PTR [Bx] (✓)

→ push CS (✓) → هيا لم يغير محتوى CS

* Hint

22h can be put in memory 25

① Byte [22h]

② word [00 22]

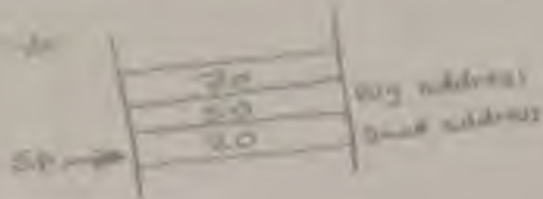
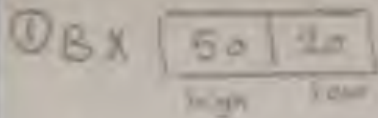
③ Dword [00 00 22]

Pop ← stack of data

Pop 2345 ← (X)

Pop CS (X) → we mustn't change CS

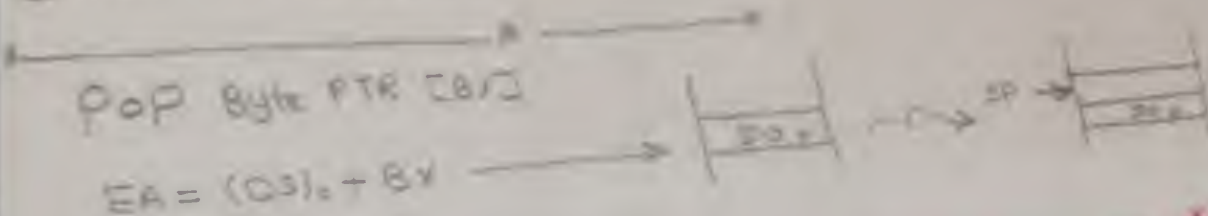
Pop BX ✓



high address → high byte

low address → low byte

② Then $SP = SP + 2$



Instructions

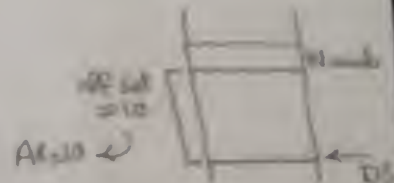
- LEA
- LDS, LSS, LFS, LGS, LES
- * off set
- LODS, STOS, MOVS, INS, OUTS
- * IN, OUT
- * XCHG
- * BSWAP
- * CMOS

→ **LEA** (load effective address)

ex: LEA AX, Numb \equiv Mov AX, off set Numb

هذا الأمر معناه وضع عدد المكان Numb من البداية في AX

ex: LEA BX, [DI] $\rightarrow EA = (DS)_0 + DI \neq$ MOV BX, off set [DI] (X)



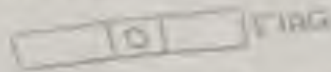
LCS EAX, [DI] (X)

because CS mustn't be changed.

String Instructions

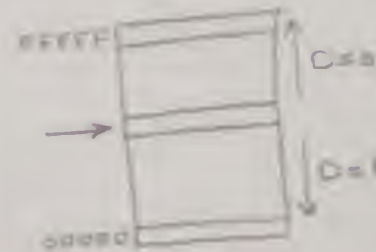
LODS, STOS, MOVS, INS, OUTS

These instructions depend on direction 0



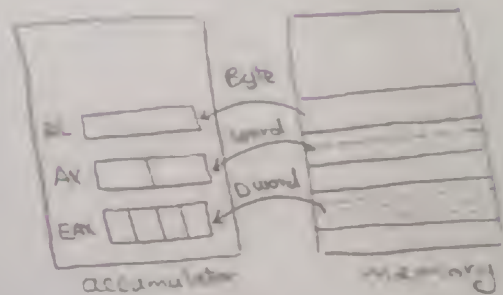
D=0 → Out of memory mode
يسير في الذاكرة / يزداد العنوان

D=1 → Out of memory mode
يسير في اتجاه نقص العنوان

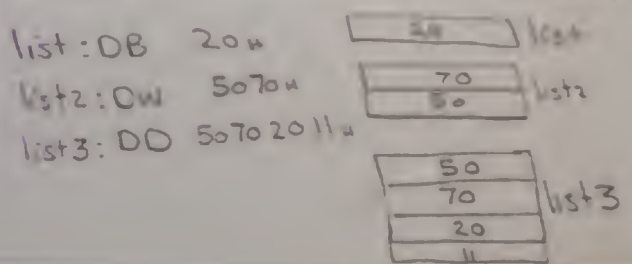


LODS

أخذ من memory ونضع في accumulator
ثم نزيد أو نقلل حسب D



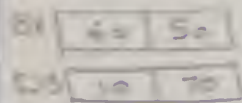
- LODSB → byte (البتة غير مفرقة مباشرة بواسطة EA عن طريق)
- LODSW → word
- LOSD → double word
- LODS list → byte (DB) (البتة لا يتم وضع قيمتها في الذاكرة مباشرة)
- LODS Data → word (DW)
- LODS FWORD → double word (DD)



→ LODS

ex: LODS BX, [DI]

$$EA = (DS)_0 + DI = \text{value}$$



Shift

byte
bit = 2

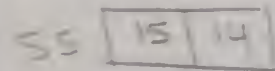
يتم قراءة البتة من الذاكرة
من الذاكرة إلى الذاكرة
في الذاكرة BX
في الذاكرة BX
في الذاكرة BX
في الذاكرة BX

في الذاكرة BX
في الذاكرة BX
في الذاكرة BX
في الذاكرة BX

→ LSS

ex: LSS EAX, [BX+DI]

$$EA = (DS)_0 + BX + DI = \text{value}$$



→ LES

ex: LES BX, [DI]

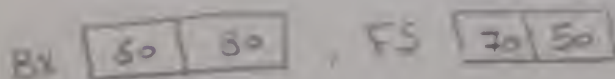
$$EA = (DS)_0 + DI = \text{value}$$



→ LFS

ex: LFS BX, [DI]

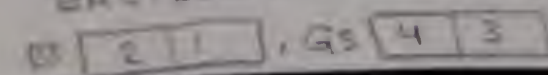
$$EA = (DS)_0 + DI = \text{value}$$

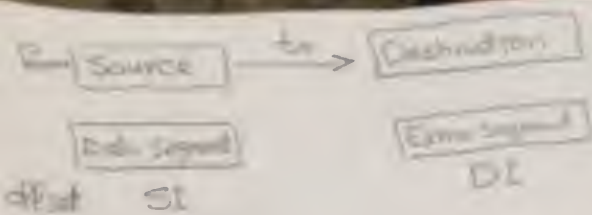


→ LGS

ex: LGS BX, [DI]

$$EA = (DS)_0 + DI = \text{value}$$





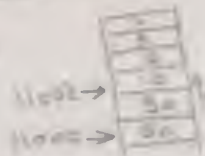
ex: DS=10000, SI=10000, D=0
execute LODSW then LODSD

Solution

$$EA = 10SI_{16} + SI = 10000 + 10000 = 11000$$

$$SI_{new} = SI_{old} + 2 \text{ bit} = 10002$$

AX [50 | 50]



To execute LODSD

$$SI = 10002, DS = 10000, D = 0$$

$$EA = 10000 + 10002 = 11002$$

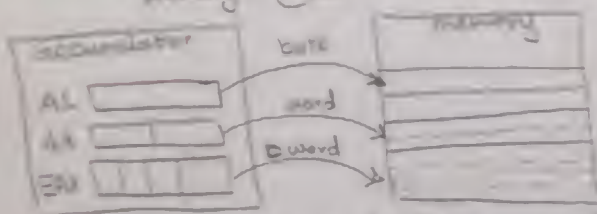
EAX [7 | 6 | 5 | 0]

$$SI_{new} = SI_{old} + 4 \text{ bit} = 10002 + 4 = 10006$$

IF D=1 $SI_{new} = SI_{old} - 1$
1 → left
2 → right
4 → down

STOS

من الaccumulator وضع في memory



تزيد offset أو قلله حسب C

STOSB, STOSW, STOSD

STOS list (DB), STOS list2 (DW)

STOS list2 (DD)

MOVZX

تزيد البايت فناناً
Zero, Zero

MOVSX

تزيد باقي المساحة
بفرض القيمة في الاشارة

4) XCHG
بدل المحتاكن
→ Both place must have the same size
→ CS mustn't be change

Examples:

XCHG AL, CL (✓)
XCHG CX, BP (✓)
XCHG EAX, AX (✓)
XCHG DS, ES (X)
XCHG CS, AX (X)

BSWAP

→ work only with 32 bit registers
EAX → P3, P47

EAX [50 | 20 | 30 | 40] before

EAX [40 | 30 | 20 | 50] after

CMOV (Conditional Move)

نقل حسب شرط

CMOVZ → هذا الأمر مفيد
1. يري حالة Z في flag
2. 0 = Z لا ينقل شيء
1 = Z ينقل

ex: CMOVZ AX, BX

IF Z=1 ∴ AX = BX

else Do nothing

→ CMOVC → check Carry

IF C=1 → Move

else Do nothing

→ CMOVNC → check No Carry

IF C=0 → Move

else Do nothing